IN THE CLAIMS

Please kindly amend the pending claims 16-35 as follows:

16. (*Currently amended*) A method of forming a CMOS image sensor, the method comprising:

forming a substrate with a first layer being a first conductive type of a semiconductor material and a second layer; ~~and~~

~~forming a layer on top of the substrate, the layer~~ being a second conductive type, the second layer being on top of the first layer and fully covering the first layer so as to form a junction therebetween that prevents substrate noise diffused into photo elements ~~formed above the layer~~ when a first voltage is applied to the ~~substrate~~ first layer and a second voltage is applied to the second layer, wherein the junction is reversely biased, and

wherein the CMOS image sensor is integrated with accessory CMOS circuits to facilitate the CMOS image sensor to operate as desired.

17. (*Previously added*) The method as in claim 16, wherein the junction is so formed to be a substrate noise barrier in the CMOS image sensor.

18. (*Currently amended*) The method as in claim 16, further comprising:

forming a deep well of the second conductive type in the second layer to prevent latch-up between the accessory CMOS circuits and the first layer~~substrate~~.

19. (*Currently amended*) The method as in claim 16, further comprising:

forming a photodiode element, the photodiode element having a first well region of the first conductive type formed in the second layer of the second conductive type; and

causing a second well region of the second conductive type to be formed in the second layer of the second conductive type with higher doping density than that of the second layer of the second conductive type.

20. (*Previously added*) The method as in claim 19, wherein the second well surrounds the first well region to form a lateral PN junction.

21. (*Currently amended*) The method as in claim 20, wherein the first well region and the second layer of the second conductive type forms a vertical PN junction.

22. (*Previously added*) The method as in claim 21, wherein both the lateral PN junction and vertical junction are reversely biased.

23. (*Previously added*) The method as in claim 16, wherein a distance between a micro-lens and a photo element in the CMOS image sensor is reduced by adding an extra process of chemical mechanical polishing (CMP) to eliminate a conventional planarization layer such that sensitivity of the photo element is increased.

24. (*Currently amended*) The method as in claim 16, further comprising:
forming a deep well of the second conductive type in the second layer to prevent latch-up between the accessory CMOS circuits and the first layer~~substrate~~, and
wherein the deep well is formed at a center depth in a range of 0.5um to 2um for a thickness in a range of 0.5 um to 2um with the second conductive type doping outside the photo element to prevent the latch-up to happen.

25. (*Currently amended*) The method as in claim 16, further comprising:
growing a top oxide layer on top of the second layer; and
carrying out a process of chemical mechanical polishing (CMP).

26. (*Currently amended*) The method as in claim 16,
wherein the ~~substrate~~ first layer is of N type, and the second layer is of P type, and

wherein the first voltage is higher than the second voltage.

27. (*Currently amended*) The method as in claim 16,
wherein the first layer ~~substrate~~ is of P type, and the second layer is of N type; and
wherein the first voltage is lower than the second voltage

28. (*Currently amended*) A CMOS image sensor comprising:
a substrate including a first layer being ~~of~~ a first type of a semiconductor material and a second layer ;
~~a layer~~ being a second type of a semiconductor material disposed on top of the ~~substrate~~ first layer and fully covering the first layer to form a junction that prevents substrate noise diffused to photo elements ~~formed above the layer~~ when a first voltage is applied to the ~~substrate~~ first layer and a second voltage is applied to the second layer, wherein the junction is reversely biased, and
wherein the CMOS image sensor is integrated with accessory CMOS circuits to facilitate the CMOS image sensor to operate.

29. (*Previously added*) The CMOS image sensor of claim 28, wherein the junction is so formed to be a substrate noise barrier that prevents substrate noise diffused into other photo elements in the CMOS image sensor.

30. (*Currently amended*) The CMOS image sensor of claim 29, wherein a deep well of the second conductive type is formed in the second layer to prevent latch-up between the accessory CMOS circuits and the ~~substrate~~first layer.

31. (*Currently amended*) The CMOS image sensor of claim 28 the ~~substrate~~ first layer is of N type, and the second layer is of P type, and wherein the first voltage is higher than the second voltage.

32. (*Currently amended*) The CMOS image sensor of claim 31, wherein a deep well of P type is formed in the second layer to prevent latch-up between wells to form a photo element and the ~~substrate~~first layer.

33. (*Currently amended*) The CMOS image sensor of claim 28, wherein the ~~substrate~~ first layer is of P type, and the second layer is of N type, and wherein the first voltage is lower than the second voltage.

34. (*Currently amended*) The CMOS image sensor of claim 33, wherein a deep well of N type is formed in the second layer to prevent latch-up between wells to form a photo element and the ~~substrate~~first layer.

35. (*Previously added*) The CMOS image sensor of claim 28, wherein a distance between a micro-lens and one of the photo diodes is reduced by adding an extra process of chemical mechanical polishing (CMP) to eliminate a conventional planarization layer such as a sensitivity of the one of the photo diodes is increased.